

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
10 June 2004 (10.06.2004)

PCT

(10) International Publication Number
WO 2004/049295 A1

(51) International Patent Classification⁷: G09G 3/36

(21) International Application Number:
PCT/IB2003/005214

(22) International Filing Date:
18 November 2003 (18.11.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
02102642.2 25 November 2002 (25.11.2002) EP

(71) Applicant (for all designated States except US): KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants (for US only): DAUM, Martin

[CH/DE]; c/o Philips Intellectual Property & Standards GmbH, Weissshausstr. 2, 52066 Aachen (DE). BUCHSCHACHER, Pascal [CH/DE]; c/o Philips Intellectual Property & Standards GmbH, Weissshausstr. 2, 52066 Aachen (DE).

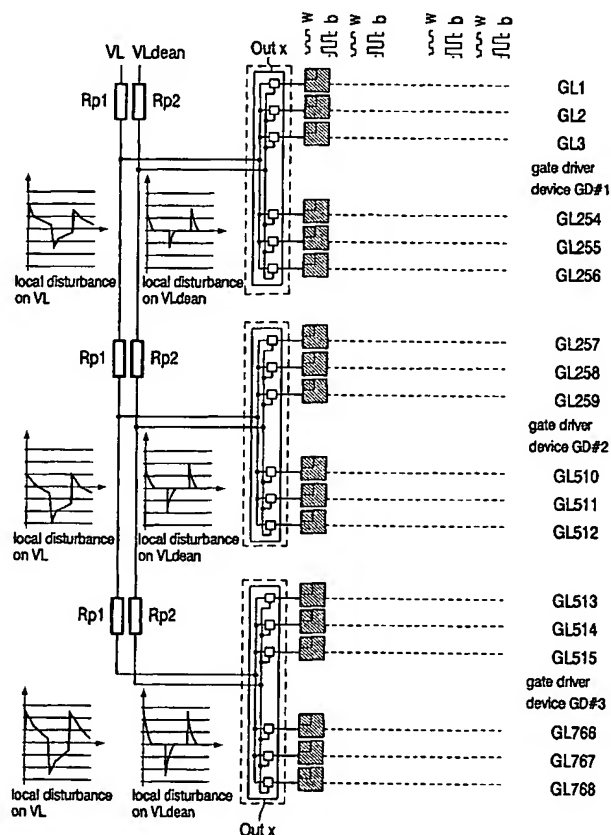
(74) Agent: MEYER, Michael; Philips Intellectual Property & Standards GmbH, Weissshausstr. 2, 52066 Aachen (DE).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

[Continued on next page]

(54) Title: DISPLAY WITH REDUCED "BLOCK DIM" EFFECT



(57) Abstract: The present invention is directed in general to a LCD-panel, and particularly to a LCD panel whose gate drivers (GD) are assembled without a printed circuit board (PCB). This technique is so called PCB-less, where the wiring of the gate drivers (GD) is not done with conventional printed circuit boards (PCB), but directly on the LCD-glass. The invention is also applicable for chip on glass (COG) technique, where the gate drivers (GD) are directly connected to the glass wiring. To avoid the block-dim effects, while keeping the effort and cost low, it is proposed to add an additional line (VLclean) to each output stage (OUTx), whereby the additional line (VLclean) is used solely for supplying the reference potential of the storage capacitors (Cst) of the selected gate line (GLy). All other (unselected) gate lines are connected to the usual gate off supply line (VL). The VLclean line is routed as a separate track on the LCD-glass and is connected to VL supply at the glass edge or close to the power-supply's output.